Impedance Characterization of GaAs FET Switches

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Abstract—**The FET switch is a very complicated device to analyze all characteristics at the same time because of the existence of nonlinearity, three-dimensional electrodes, passivation layers, and depletion regions. Since the GaAs FET switch can be regarded as a linear small-signal device in the on- and off-state, a linear analysis is carried out in this paper only of the two states but by taking into account the geometry of electrodes, passivation layers, and depletion regions. The rectangular boundary division method is applied to solve Laplace's equation for the impedance characterization of GaAs FET switches. Equivalent electrical circuits composed of capacitors and resistors are defined for the on-state and off-state of a FET switch. The capacitances and resistances in the equivalent circuits are estimated and compared with experimentally measured values at 10 GHz. The quality factor of the FET switch, which can be used for estimating insertion loss, is calculated by using the two equivalent series impedances of the FET switch corresponding to the two states.**

I. Introduction

DURING the recent progress of monolithic microwave integrated circuits (MMIC) technology, MMIC phase shifters and switches have been widely investigated for active phased array radars [1]. Since the GaAs Field Effect Transistor (FET) is a basic circuit component in MMIC's, it is mostly used as a switching element in MMIC phase shifters replacing the role of p-i-n diodes used in MIC circuits. GaAs FET's switch between the on- and the off-states following the changes in the depletion region occurring with changes in the gate bias voltage. The GaAs FET switch in either state can be regarded as a linear device for small-signals. The capacitances and the resistances in an equivalent circuit can therefore be evaluated based on Laplace's equation. The switching performance, the switching quality factor defined by Kurokawa, and the power handling capability of a GaAs FET switch with the knowledge of breakdown voltage can be then estimated by using such equivalent circuits.

GaAs FET switch control devices have been described using various models in the past [2]–[6]. Takada *et al.* introduced a GaAs FET capacitance model [3] and Alexopoulos *et al.* expressed a GaAs FET electrode capacitance matrix using a Green's function technique [4]. Their GaAs FET models are, however, too simple to describe the majority of actual devices. Though such simplified versions of the switch structure model have been analyzed in the past, all the complication of their electrodes and passivation layers have never been rigorously taken into account either in the analysis to estimate capacitances and resistances or in the estimation of the effects of the depletion region on device characteristics. This is perhaps because of analytical difficulty. Those neglected factors in the past, however, are not really negligible as discussed in this paper.

This paper describes firstly the application of the rectangular boundary division method [7] to the analysis of the electric potential distribution and of the current distribution in a given FET device with particular electrode, passivation layer, and depletion region structures, and secondly the estimation method of the capacitances and resistances in equivalent circuits for the on-state and the off-state of the FET switch. The quality factor of the GaAs FET switch is also estimated by using the equivalent circuits in order to conveniently describe the switching performance.

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II. Analysis Method

Fig. 1 shows the cross-sectional view of a GaAs FET used for MMIC switches. The active n-layer and the contact n^+-layer are made by the ion-implantation technique. The gate electrode is formed at the center of the active n-layer, and the drain and the source electrodes on the n^+-layer. The passivation layers consisting of SiO_2 and Si_3N_4 are fabricated on the GaAs surface. When making device models, account must be taken of effect of these passivation layers in addition to that of the active n and n^+ layers.

Fig. 2 shows two equivalent circuits for the on-state and off-state of the GaAs FET switch. When the GaAs FET is used as a switching element, dc bias voltages are usually not applied to the drain and source electrode. Only gate bias voltage is applied to the FET to switch from the on-state to the off-state or vice versa. Since no gate bias voltage needs to be applied for the on-state (for depletion mode FETs), the resistance between the drain and the source is fixed within small values as shown in Fig. 2. To transfer the switch to its off-state gate, voltages equal to or beyond the pinch-off voltage are applied to the FET.

Since the FET is regarded as a small-signal linear device when only the on-state and off-state are concerned, the total electric field energy in the FET can be easily formulated by the potential distribution and current distribution obtained by solving Laplace's equation. The problem of finding switching properties between the on-

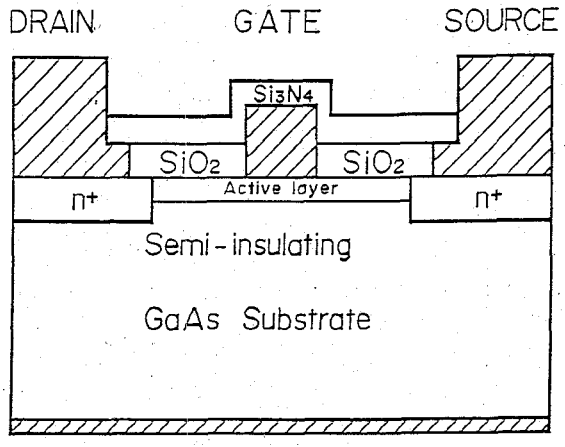

Fig. 1. Cross-sectional view of a GaAs FET to be analyzed.

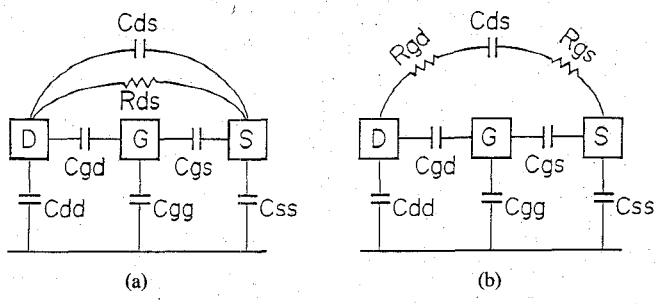

Fig. 2. GaAs FET equivalent circuits. (a) On-state. (b) Off-state.

state and off-state is, therefore, reduced to the problem of obtaining the two equivalent circuits of the FET corresponding the two states.

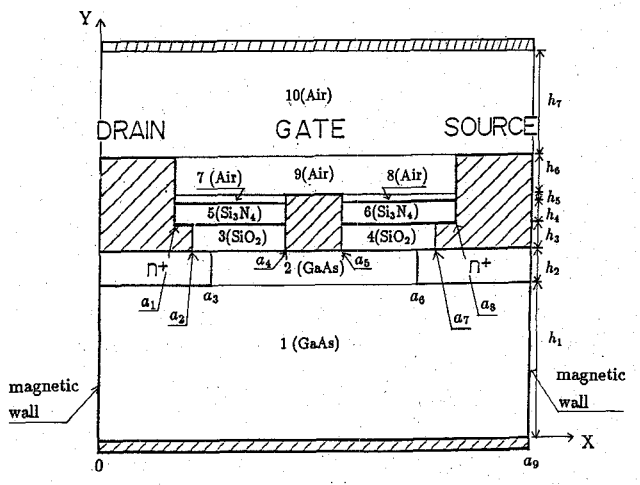

Fig. 3. Ten small regions with rectangular boundaries. $L_g = a_5 - a_4 = 0.7$; $L_{ds} = a_6 - a_3 = 4.0$; $a_7 - a_2 = 6.0$; $a_8 - a_1 = 8.0$; $a_9 = 28.0$; $h_1 = 150$; $h_2 = 0.5$; $h_3 = 0.3$; $h_4 = 0.2$; $h_5 = 0.15$; $h_6 = 0.35$; $h_7 = 15\,000.0$ [unit; μm]; $\epsilon_1 = \epsilon_2 = 12.7$ (GaAs); $\epsilon_3 = \epsilon_4 = 4.5$ (SiO_2); $\epsilon_5 = \epsilon_6 = 7.0$ (Si_3N_4); $\epsilon_7 = \epsilon_8 = \epsilon_9 = \epsilon_{10} = 1.0$ (air).

A. Equivalent Capacitors

Fig. 3 shows the cross-sectional view of the GaAs FET divided into 10 small rectangular regions to apply the rectangular boundary division method. The most of the passivation layer (Si_3N_4) regions are taken into account in our analysis. The capacitance values of the equivalent circuits can be estimated by using the relation between the total electric field energy and the energy stored in a capacitor.

In the rectangular boundary division method, the potential function for each region is expressed in the Fourier series form so as to satisfy Laplace's equation subject to boundary conditions on two side-walls in each subregion as follows:

$$\phi_1(x, y) = \frac{A_{10}}{h_1} y + \sum_{n=1}^{\infty} A_{1n} \sinh(\zeta_{1n} y) \cos(\zeta_{1n} x) \qquad \text{(Region 1; } 0 \le x \le a_9,\ 0 \le y \le h_1\text{)} \tag{1a}$$

$$\phi_2(x, y) = \frac{a_6 - x}{a_6 - a_3} V_D + \frac{x - a_3}{a_6 - a_3} V_S + \sum_{n=1}^{\infty} [A_{2n} \sinh(\zeta_{2n} y) + B_{2n} \cosh(\zeta_{2n} y)] \sin(\zeta_{2n}(x - a_3))$$

$$\text{(Region 2; } a_3 \le x \le a_6,\ h_1 \le y \le h_1 + h_2\text{)} \tag{1b}$$

$$\phi_3(x, y) = \frac{a_4 - x}{a_4 - a_2} V_D + \frac{x - a_2}{a_4 - a_2} V_G + \sum_{n=1}^{\infty} [A_{3n} \sinh(\zeta_{3n} y) + B_{3n} \cosh(\zeta_{3n} y)] \sin(\zeta_{3n}(x - a_2))$$

$$\text{(Region 3; } a_2 \le x \le a_4,\ h_1 + h_2 \le y \le h_1 + h_2 + h_3\text{)} \tag{1c}$$

$$\phi_4(x, y) = \frac{a_7 - x}{a_7 - a_5} V_G + \frac{x - a_5}{a_7 - a_5} V_S + \sum_{n=1}^{\infty} [A_{4n} \sinh(\zeta_{4n} y) + B_{4n} \cosh(\zeta_{4n} y)] \sin(\zeta_{4n}(x - a_5))$$

$$\text{(Region 4; } a_5 \le x \le a_7,\ h_1 + h_2 \le y \le h_1 + h_2 + h_3\text{)} \tag{1d}$$

$$\phi_5(x, y) = \frac{a_4 - x}{a_4 - a_1} V_D + \frac{x - a_1}{a_4 - a_1} V_G + \sum_{n=1}^{\infty} [A_{5n} \sinh(\zeta_{5n} y) + B_{5n} \cosh(\zeta_{5n} y)] \sin(\zeta_{5n}(x - a_1))$$

$$\text{(Region 5; } a_1 \le x \le a_4,\ h_1 + h_2 + h_3 \le y \le h_1 + h_2 + h_3 + h_4\text{)} \tag{1e}$$

$$\phi_6(x, y) = \frac{a_8 - x}{a_8 - a_5} V_G + \frac{x - a_5}{a_8 - a_5} V_S + \sum_{n=1}^{\infty} [A_{6n} \sinh(\zeta_{6n} y) + B_{6n} \cosh(\zeta_{6n} y)] \sin(\zeta_{6n}(x - a_5))$$

$$(\text{Region 6; } a_5 \le x \le a_8,\ h_1 + h_2 + h_3 \le y \le h_1 + h_2 + h_3 + h_4) \tag{1f}$$

$$\phi_7(x, y) = \frac{a_4 - x}{a_4 - a_1} V_D + \frac{x - a_1}{a_4 - a_1} V_G + \sum_{n=1}^{\infty} [A_{7n} \sinh(\zeta_{7n} y) + B_{7n} \cosh(\zeta_{7n} y)] \sin(\zeta_{7n}(x - a_1))$$

$$(\text{Region 7; } a_1 \le x \le a_4,\ h_1 + h_2 + h_3 + h_4 \le y \le h_1 + h_2 + h_3 + h_4 + h_5) \tag{1g}$$

$$\phi_8(x, y) = \frac{a_8 - x}{a_8 - a_5} V_G + \frac{x - a_5}{a_8 - a_5} V_S + \sum_{n=1}^{\infty} [A_{8n} \sinh(\zeta_{8n} y) + B_{8n} \cosh(\zeta_{8n} y)] \sin(\zeta_{8n}(x - a_5))$$

$$(\text{Region 8; } a_5 \le x \le a_8,\ h_1 + h_2 + h_3 + h_4 \le y \le h_1 + h_2 + h_3 + h_4 + h_5) \tag{1h}$$

$$\phi_9(x, y) = \frac{a_8 - x}{a_8 - a_1} V_D + \frac{x - a_1}{a_8 - a_1} V_S + \sum_{n=1}^{\infty} [A_{9n} \sinh(\zeta_{9n} y) + B_{9n} \cosh(\zeta_{9n} y)] \sin(\zeta_{9n}(x - a_1))$$

$$(\text{Region 9; } a_1 \le x \le a_8,\ h_1 + h_2 + h_3 + h_4 + h_5 \le y \le h_1 + h_2 + h_3 + h_4 + h_5 + h_6) \tag{1i}$$

$$\phi_{10}(x, y) = \frac{A_{100}}{h_7}(b - y) + \sum_{n=1}^{\infty} A_{10n} \sinh(\zeta_{10n}(b - y)) \cos(\zeta_{10n} x)$$

$$(\text{Region 10; } 0 \le x \le a_9,\ h_1 + h_2 + h_3 + h_4 + h_5 + h_6 \le y \le h_1 + h_2 + h_3 + h_4 + h_5 + h_6 + h_7 = b) \tag{1j}$$

where

$$\zeta_{1n} = \frac{n\pi}{a_9},\quad \zeta_{2n} = \frac{n\pi}{a_6 - a_3},\quad \zeta_{3n} = \frac{n\pi}{a_4 - a_2},$$

$$\zeta_{4n} = \frac{n\pi}{a_7 - a_5},\quad \zeta_{5n} = \frac{n\pi}{a_4 - a_1},$$

$$\zeta_{6n} = \frac{n\pi}{a_8 - a_5},\quad \zeta_{7n} = \frac{n\pi}{a_4 - a_1},\quad \zeta_{8n} = \frac{n\pi}{a_8 - a_5},$$

$$\zeta_{9n} = \frac{n\pi}{a_8 - a_1},\quad \zeta_{10n} = \frac{n\pi}{a_9} \tag{1k}$$

where V_D, V_G, and V_S are the given potentials to the drain, the gate, and the source electrode. These Fourier coefficients are given after specifying potential functions on the boundary.

When the Fourier coefficients are determined so as to minimize the total electric field energy, those coefficients should be the best choice. The Rayleigh–Ritz procedure using each Fourier coefficient as a variable, therefore, can be considered as one way to minimize the total field energy. However, this procedure is numerically inefficient because an infinite number of the Fourier series coefficients exist and the convergence of the Fourier series is usually slow.

We found an efficient method to minimize the total field energy, namely, we use boundary potentials as trial functions. Specifically, we adopt the first order spline function to express the boundary potentials because this function can easily describe a variety of functions using only a small number of parameters. The potential distribution on the boundary $y = h_1$, for instance, is then expressed in the following form:

$$f(x, h_1) = \begin{cases} V_D & (0 \le x \le a_3) \\ \sum_{i=0}^{m_1} F_i(x) & (a_3 \le x \le a_6) \\ V_S & (a_6 \le x \le a_9) \end{cases} \tag{2}$$

where

$$F_i(x) = \begin{cases} \dfrac{p_i - p_{i+1}}{b_i - b_{i+1}}(x - b_{i+1}) + p_{i+1} \\ \qquad (b_i \le x \le b_{i+1}) \\ 0 \quad (\text{elsewhere}). \end{cases} \tag{3}$$

Once the potential for each spline-knot on the boundary is given, the Fourier coefficients can be determined. The total electric field energy is then given in the following form:

$$U = \sum_{\nu=1}^{10} \frac{1}{2} \epsilon_\nu \epsilon_0 \iint_{S_\nu} \left[\left(\frac{\partial \phi_\nu}{\partial x} \right)^2 + \left(\frac{\partial \phi_\nu}{\partial y} \right)^2 \right] dx\, dy \tag{4}$$

where ϵ_ν, S_ν, and ϵ_0 denote the dielectric constant and the cross-sectional area of the region ν ($\nu = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10$), and the permittivity in vacuum, respectively.

The above total electric field energy can be systematically minimized by varying the potentials at each spline-knot. The other boundary condition, the continuation of the normal component of the electric flux density, is automatically satisfied when taking the minimum of the total electric field energy. This minimization procedure even-

tually results in a set of inhomogeneous linear equations on the spline-knot potentials as variables [7].

The solutions of these linear equations determine the potential distribution on each boundary. When the structure as shown in Fig. 3 is symmetrical, the capacitances of the four equivalent capacitors, *Cgs* (= *Cgd*), *Cds*, *Cgg* and *Cdd* (= *Css*), are determined by specifying the four combinations of voltages to each electrode as shown in Table I. The capacitances in the equivalent circuit are obtained by solving these linear equations. The total device capacitances are estimated by multiplying these capacitances (per unit length) by the gate width.

Fig. 4 shows the cross-sectional view of the GaAs FET for the case where the device is in the pinch-off state. When the impurity density distribution is assumed to be a step function, the width of the depletion region L_d is given by

$$L_d = L_g + 2L_e \tag{5}$$

where L_g is the gate length and L_e is the channel height given by

$$L_e = \sqrt{\frac{\epsilon_r \epsilon_0 (\phi + V)}{q n_d}} \tag{6}$$

where q denotes the electronic charge, ϕ the built-in potential, V the reverse bias voltage, n_d the ion density in the depletion region. ϵ_r the dielectric constant of GaAs material. The active layer except the depletion region is treated as a conductor electrode. The undepleted area is regarded as a resistor element.

The active current in the depletion region is cut off in the off-state due to the reverse bias voltage applied to the gate electrode. The gate electrode potential in the on-state is zero. The n^+-buffer-layer in either state should be treated as a conductor electrode.

B. Equivalent Resistors

Fig. 5 shows the on-state current distribution model for the GaAs FET. The drain electrode potential is equal to the dc source electrode potential in the on-state. When RF signals are applied to the FET switch, the drain electrode voltage is positive and the source electrode voltage is null. Therefore, the current flows from the drain to the source in the active layer. Since the conductivities of the passivation layer, the semi-insulating GaAs substrate, and the depletion region except the active layer as shown in Fig. 5(a) are very small, the current dose not flow in these regions.

The condition at boundaries between the conductive region and non-conductive one is given by

$$\frac{\partial \phi_\nu}{\partial n} = 0 \tag{7}$$

where n denotes the normal coordinate to the surface and ϕ is the potential in the region ν (ν = 1, 2, 3). We again apply the rectangular boundary division method to estimate the current distribution in the model as shown in Fig. 5(a) taking into account these facts. Fig. 5(b) shows the dimensions of the three regions with rectangular boundaries.

TABLE I
RELATION BETWEEN ENERGY AND CAPACITANCE

V_D	V_G	V_S	Relation Between Energy and Capacitance
1	0	1	$2W_{101} = 2Cgs + 2Cdd$
0	1	0	$2W_{010} = 2Cgs + Cgg$
1	0	0	$2W_{100} = Cgs + Cds + Cdd$
1	1	1	$2W_{111} = 2Cdd + Cgg$

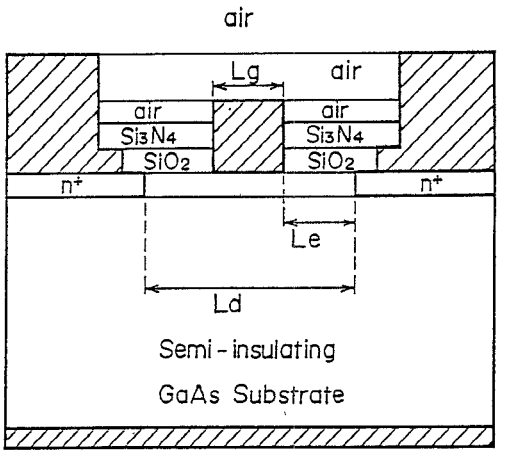

Fig. 4. GaAs FET switch in the off-state.

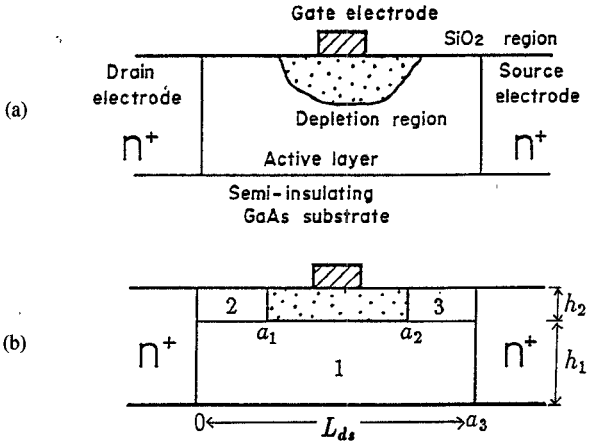

Fig. 5. GaAs FET switch resistance model for the on-state. (a) Physical structure. (b) Divided rectangular regions.

The potential function for each region is given in the Fourier series form as follows:

$$\phi_1(x, y) = \frac{x}{a_3} V_S + \frac{a_3 - x}{a_3} V_D + \sum_{n=1}^{\infty} A_{1n} \cosh(\zeta_{1n} y) \sin(\zeta_{1n} x)$$

(Region 1; $0 \le x \le a_3$, $0 \le y \le h_1$) (8-a)

$$\phi_2(x, y) = V_D + \sum_{n=1}^{\infty} A_{2n} \cosh(\zeta_{2n}(b - y)) \sin(\zeta_{2n}x)$$

(Region 2; $0 \le x \le a_1$, $h_1 \le y \le h_1 + h_2 = b$) (8-b)

$$\phi_3(x, y) = V_S + \sum_{n=1}^{\infty} A_{3n} \cosh(\zeta_{3n}(b - y)) \cdot \sin(\zeta_{3n}(x - a_2))$$

(Region 3; $a_2 \le x \le a_3$, $h_1 \le y \le h_1 + h_2 = b$) (8-c)

where

$$\zeta_{1n} = \frac{n\pi}{a_3}, \quad \zeta_{2n} = \frac{(2n-1)}{2a_1}\pi, \quad \zeta_{3n} = \frac{(2n-1)}{2(a_3 - a_2)}\pi \tag{8-d}$$

and V_D and V_S are the drain and the source electrode potential, respectively.

The potential distribution at the surface of $y = h_1$ is approximated with the first order spline function. The total electric field energy as the sum of the energy of each region can be obtained in a similar fashion to the capacitance analysis. A set of inhomogeneous linear equations for the potentials of the spline-knots can be obtained by minimizing the total electric field energy. The solutions of these linear equations determine all the potential distribution. The minimized energy obtained with this potential distribution is related to the resistance as

$$\frac{V^2}{2R_{ds}} = \sum_{\nu=1}^{3} \frac{1}{2}\sigma_\nu \iint_{S_\nu} \left[\left(\frac{\partial \phi_\nu}{\partial x}\right)^2 + \left(\frac{\partial \phi_\nu}{\partial y}\right)^2\right] dx\, dy \tag{9}$$

where σ_ν is the conductivity of the νth layer. The resistance between the drain and the source can be estimated by this expression. The leakage resistance between the drain and the source in general is so large in the off-state that it can be neglected in the equivalent resistance circuit.

The off-state resistances, *Rgd* and *Rgs*, as shown in Fig. 6 can be similarly obtained by using the relations

$$R_{gd} = \frac{\rho S}{hw}\ [\Omega] \tag{10a}$$

and

$$R_{gs} = \frac{\rho(a - S - L_d)}{hw}\ [\Omega] \tag{10b}$$

respectively, where ρ is the resistivity of the active layer except the depletion regions and w is the total gate width.

III. Numerical and Experimental Results

A. Capacitances

The off-state capacitances were calculated for the reverse bias voltage of -5 [V]. Fig. 7 shows the good convergence property of the capacitance values against the numbers of the Fourier series terms. Fig. 8 shows the capacitance versus the width of the depletion region in the off-state. When the width of the depletion region is large, the equivalent capacitance in the off-state, *Cds*, is larger than the *Cgs* as seen in Fig. 8. Table II shows the ratio of the energy stored in the depletion region to those in other regions when applying voltages of $V_d = -1$, $V_g = 0$, $V_s = 1$ [V].

The capacitance produced by the existence of the passivation layer was found to be too large to be neglected according to our numerical results. Fig. 9 shows the capacitances versus the gate length. The computation time to obtain one capacitance value was about 140 seconds on a HITAC M260-D computer when the number of nodes was 122 and the number of the Fourier series terms was 1000.

The off-state capacitances, $C_{ds} + \frac{1}{2}C_{gs}$, were measured for the four types of FET's mounted in a microstrip resonator. Experimental values of the capacitances were estimated using a HP-8510 network analyzer. All the four FET's had the same gate length and the same carrier profiles but the different total gate width of 420 (5 fingers), 800, 1200 and 1400 (6 fingers) [μm]. The calculated capacitance values for these of FET's show good agreement with the measured ones as shown in Table III.

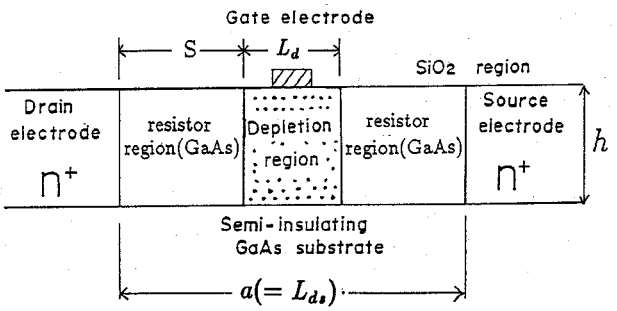

Fig. 6. GaAs FET switch resistance model for the off-state.

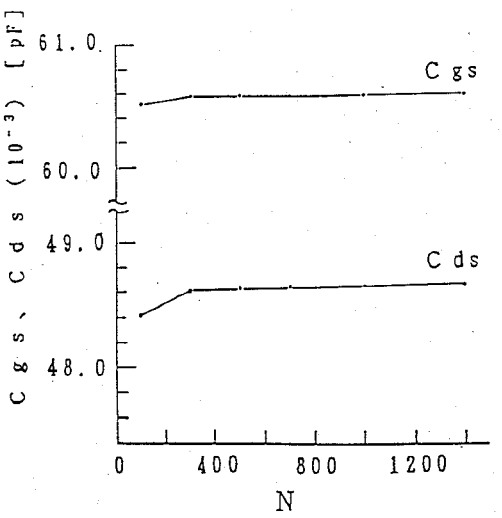

Fig. 7. Convergence of the capacitance values against the number of Fourier series terms. Total gate width $w = 320$ [μm]. $L_d = 1.18$ [μm].

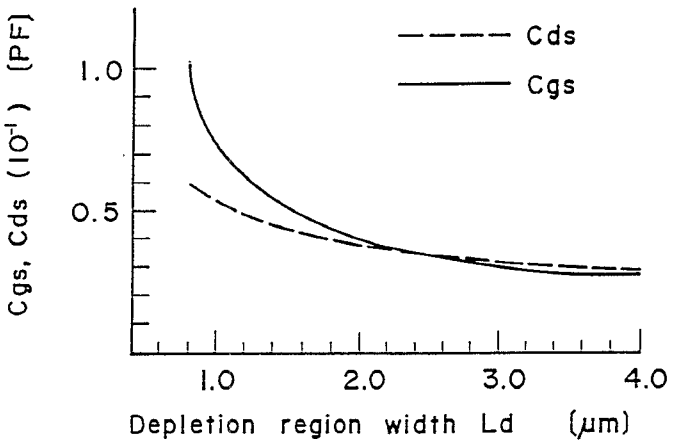

Fig. 8. The capacitance values versus the depletion region width. Total gate width $w = 320$ [μm].

TABLE II
ENERGY DISTRIBUTION TO EACH REGION

(a) Off State			(b) On-State		
Depletion region	26.8%		Depletion region	12.1%	
	73.2%			87.9%	
Other regions	Semi-insulating GaAs substrate	58.7%	Other regions	Semi-insulating GaAs substrate	77.0%
	SiO_2, Si_3N_4 Passivations	14.5%		SiO_2, Si_3N_4 Passivations	10.9%

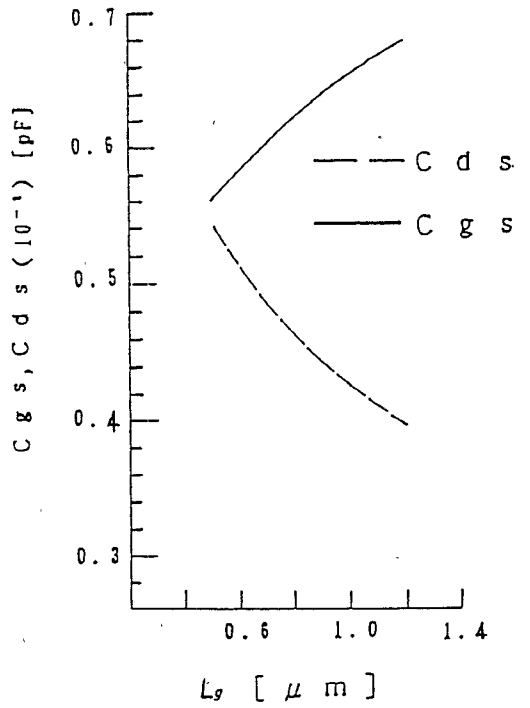

Fig. 9. The capacitance values versus the gate length. Total gate width $w = 320$ [μm]. $L_e = 0.24$ [μm].

TABLE III
FET Dimensions { gate length 0.7 (μm); doping-concentration 1.2×10^{17} (cm^{-3}) }

Total Gate Width (μm)	Measured Values (pF)	Calculated Values (pF)
420	0.102	0.102
900	0.209	0.218
1200	0.267	0.291
1400	0.325	0.339

$L_g = a_5 - a_4 = 0.7$; $L_{ds} = a_6 - a_3 = 4.0$; $a_7 - a_2 = 6.0$; $a_8 - a_1 = 8.0$; $a_9 = 28.0$; $h_1 = 150$; $h_2 = 0.5$; $h_3 = 0.3$; $h_4 = 0.2$; $h_5 = 0.15$; $h_6 = 0.35$; $h_7 = 15000.0$ [unit; μm]. $\epsilon_1 = \epsilon_2 = 12.7$ (GaAs); $\epsilon_3 = \epsilon_4 = 4.5$ (SiO_2); $\epsilon_5 = \epsilon_6 = 7.0$ (Si_3N_4); $\epsilon_7 = \epsilon_8 = \epsilon_9 = \epsilon_{10} = 1.0$ (air); $V = -5$ (V).

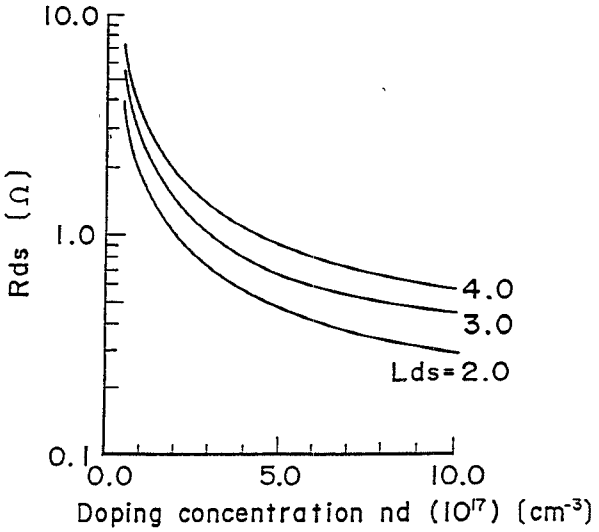

Fig. 10. The resistance between the drain and the source electrode versus the doping concentration. Total gate width $w = 320$ [μm].

B. Resistances

Fig. 10 shows the computed results of the resistance between the drain and the source in the on-state versus the impurity density in the active layer. The analysis of the on-state resistance is simple due to the simple model for current flow.

IV. Impedance of FET Switches

The equivalent switching circuits of the on-state and the off-state structure are depicted in Fig. 11(a) and (b), respectively, based on the above numerical results on the capacitance and the resistance. When a switch circuit with a single-pole single-throw (SPST) or single-pole double-throw (SPDT) [8] is designed, the on-state impedance of the switch is approximately determined by the resistance between the drain and the source of the on-state equivalent circuit and the off-state impedance is approximately given by the capacitances of the off-state equivalent circuit.

The series impedance of the FET switch thus obtained

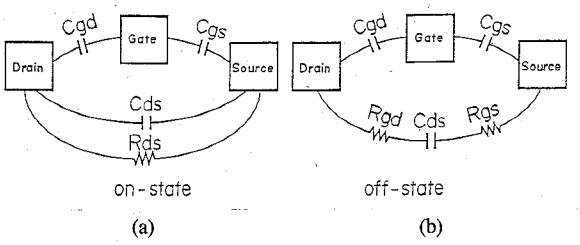

Fig. 11. The equivalent circuits of a GaAs FET switch. Total gate width $w = 320$ [μm]. $n_d = 2.0$ (10^{17}) [cm^{-3}]. (a) $C_{ds} = 0.0283$ [pF] $C_{gd} = C_{gs} = 0.0266$ [pF] $R_{ds} = 1.844$ [Ω]. (b) $C_{ds} = 0.0504$ [pF] $C_{gd} = C_{gs} = 0.0647$ [pF] $R_{gd} = R_{gs} = 0.629$ [Ω].

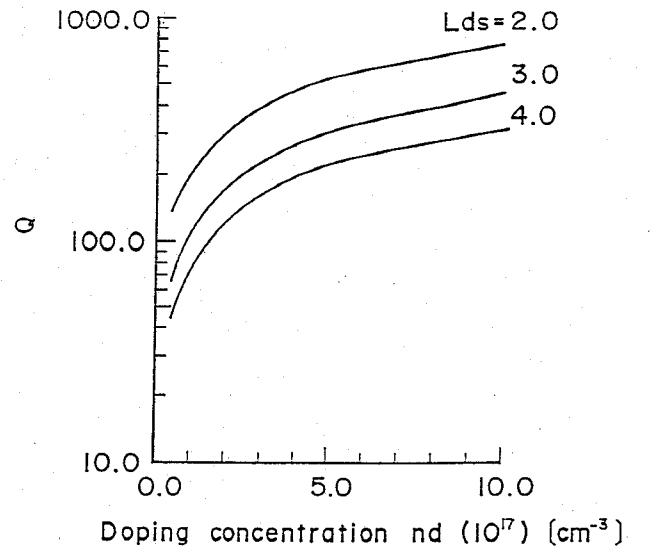

Fig. 12. Quality factor versus the doping concentration. Total gate width $w = 320$ [μm].

for the on-state is denoted by $Z_1 = R_1 + jX_1$, and that for the off-state by $Z_2 = R_2 + jX_2$.

V. Quality Factor of FET Switches

Kurokawa *et al.* defined the quality factor of the switch circuits by [9]

$$Q = \frac{\sqrt{(R_1 - R_2)^2 + (X_1 - X_2)^2}}{\sqrt{R_1 R_2}} \tag{11}$$

as one of the figure of merits to express the quality of the FET switches. The high value of Q implies low insertion loss or high isolation of the FET switch. Fig. 12 shows the calculated results of Q values versus the carrier concentration at 10 GHz. The high carrier concentration and the small spacing between the drain and the source electrode leads to a high Q factor.

VI. Conclusion

In this paper, we described an effective method for analyzing the equivalent impedance of the GaAs FET used in MMIC phase shifters and switches. This analysis includes the investigation of the effects of geometrical structures having complicated electrodes, passivation layers, and a depletion region, on capacitance and resistance values. Experimentally measured values of the off-state capacitances were found to agree well with calculated values. The on-state and off-state equivalent impedance of the FET switch were derived based on the calculated capacitance and resistance. In conclusion, we can say that the proposed analysis method is effective in various aspects to estimate the impedances corresponding to the two states and the quality factor of the FET switch from its geometrical and material configurations [10].

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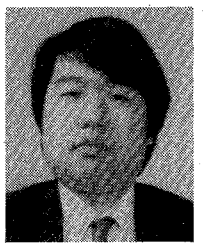

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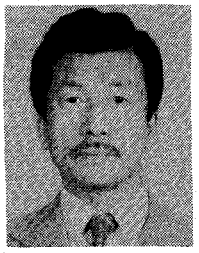

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